University of Virginia

Mixed Signal Infrastructure Circuits for Energy Autonomous Ultra Low Power Systems on Chip

PhD Proposal

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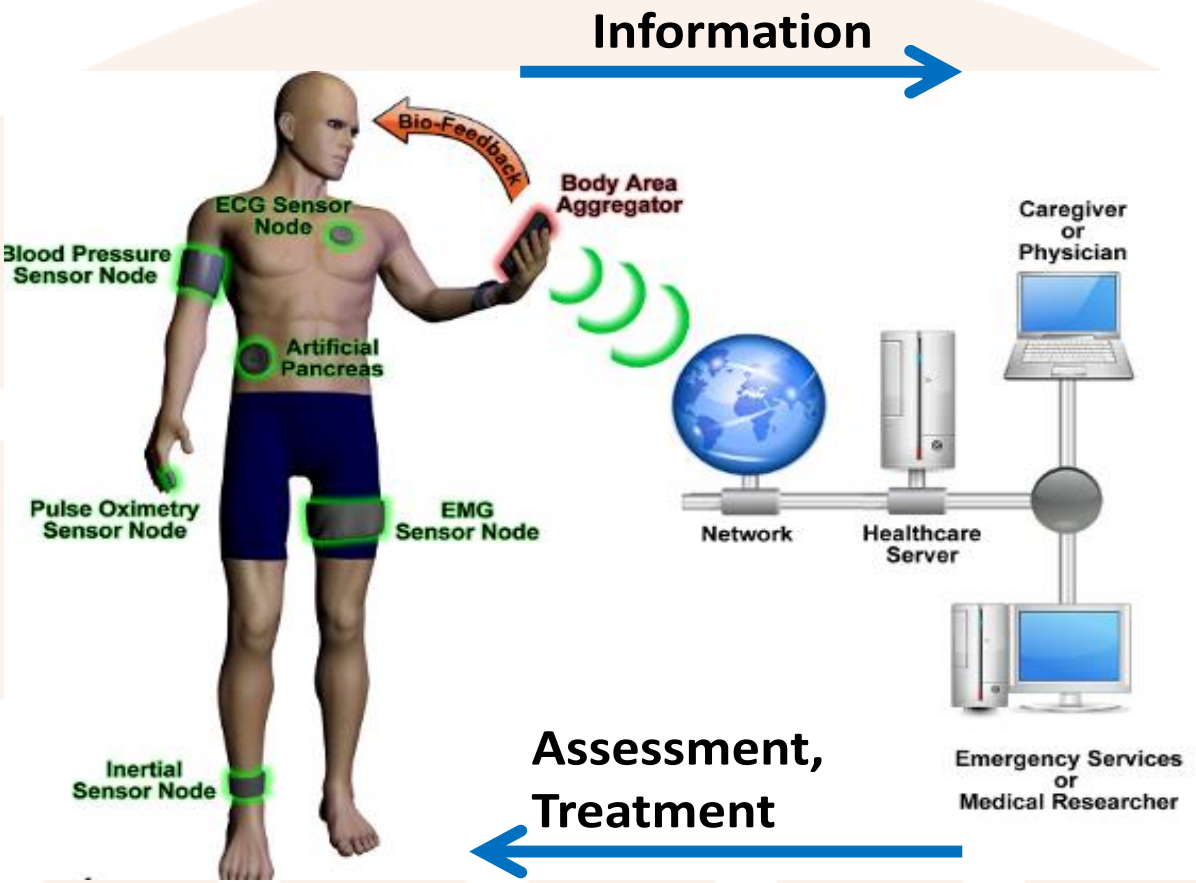
20th March 2013

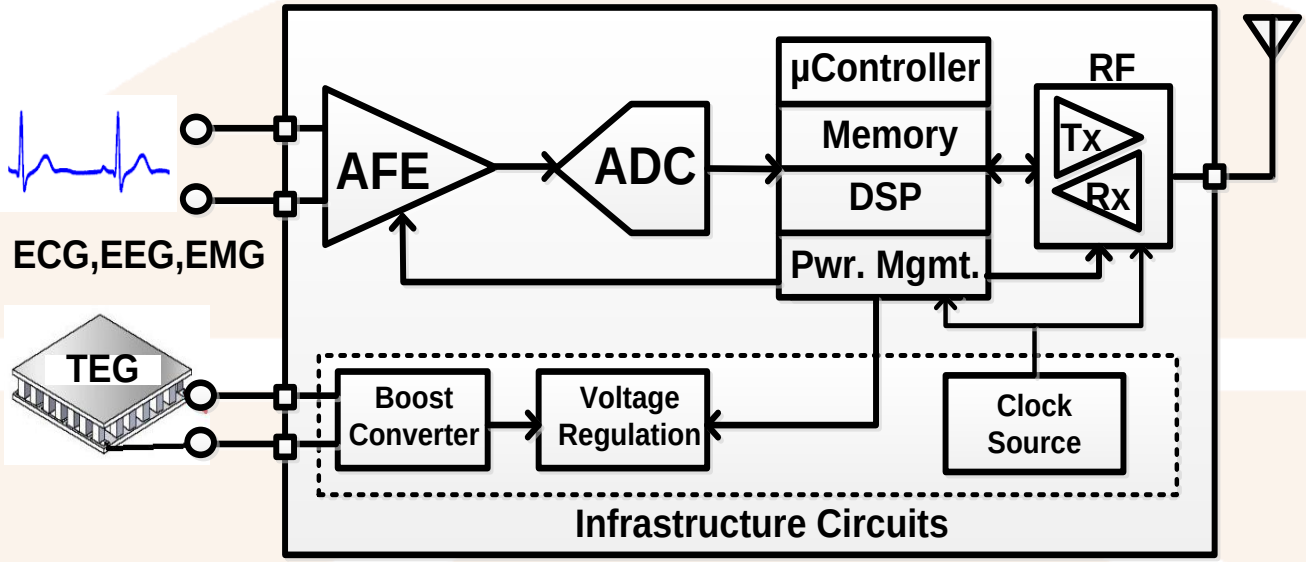
Robust Low Power VLSI

Ultra Low Power SoCs (e.g. BSN)



- BSNs promise to change the way we live
- Energy harvesting
- **Need higher life-time for ubiquitous deployment**

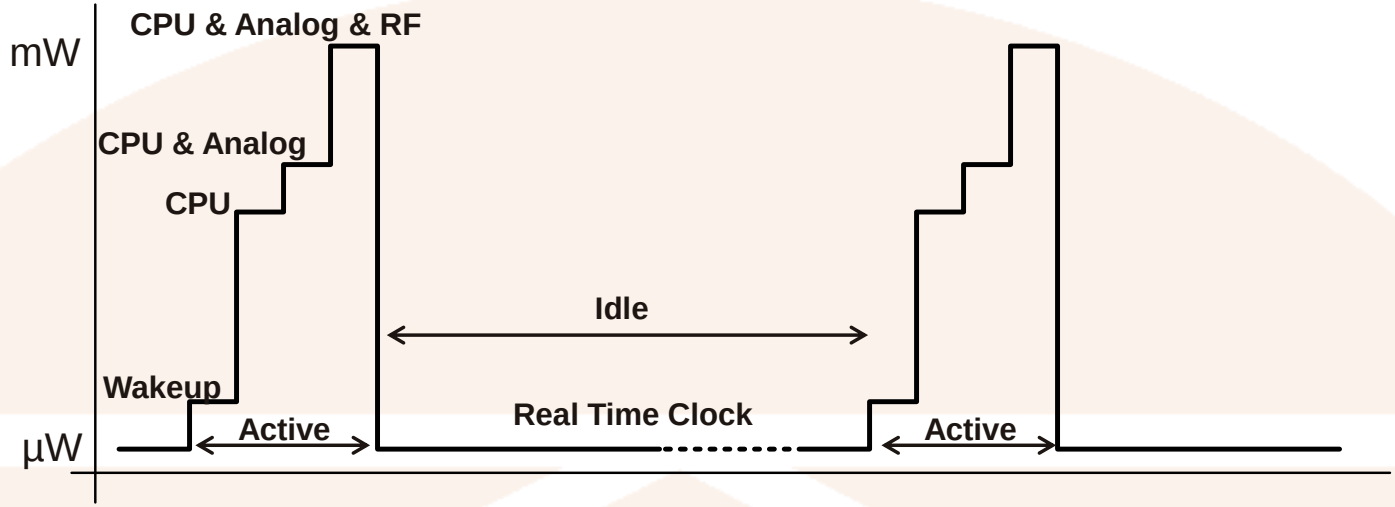
Body sensor System on Chip



Y. Zhang, et al, "A Batteryless 19uW…. ", ISSCC, Feb. 2012.

- AFE and ADC perform sensing task
- µ-controller, memory etc. perform processing
- Radio for communication
- **Infrastructure circuits- Boost converter, Regulators & Clock impact the life time of the SoC**

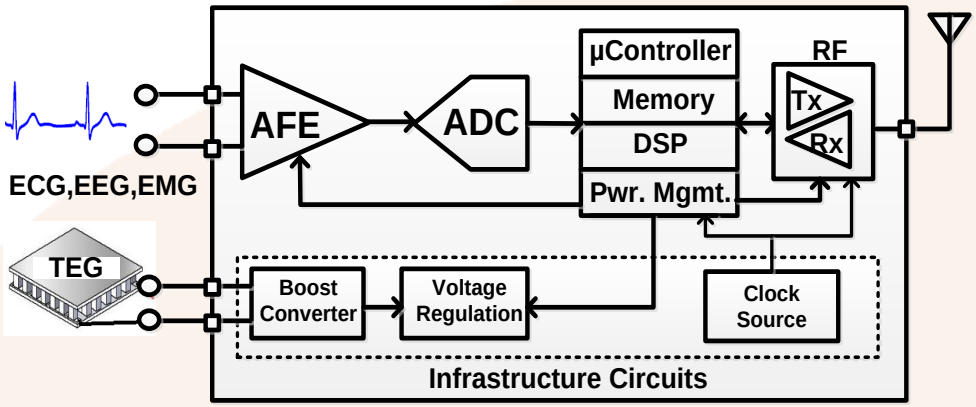
BSN Power Consumption

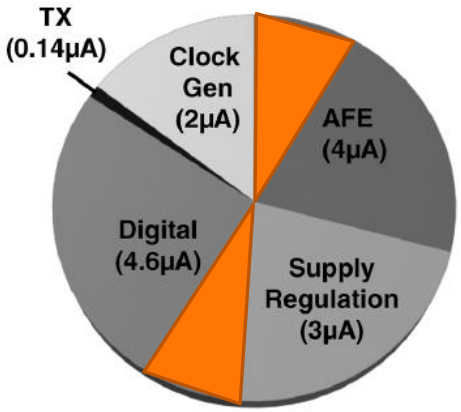


Phases	E. Harvester	Regulators	Clock	CPU	Analog	RF
Wake-up	ON	ON	ON	OFF	OFF	OFF
Processing	ON	ON	ON	ON	OFF	OFF
Sensing	ON	ON	ON	ON	ON	OFF
Communication	ON	ON	ON	ON	ON	ON
Idle/sleep	ON	ON	ON	OFF	OFF	OFF

- **Infrastructure circuits- Energy Harvester, Regulators & Clock can significantly impact the life time of the SoC**

Infrastructure circuit needs





19µW out of 50µW from TEG

Y. Zhang, et al, "A Batteryless 19uW…. ", JSSC, Jan. 2013.

- Efficient energy-harvesting (E-harvesting)
  - To increase the amount of harvested energy
- Efficient multiple regulated output voltages
  - To minimize the loss in voltage regulation
- Ultra-low power clocking scheme
  - To elongate life time in idle mode

Proposed Thesis Contributions

- **ULP clocking to reduce idle mode power**
  - Stable on-chip clocking scheme
    - Stable on-chip clock source
    - A fast locking circuit
    - ULP clock
  - ULP Crystal Oscillator
  - ULP clock and Data Recovery

- **Energy Harvesting and Power Management to increase harvested energy and reduce loss**
  - Efficient energy harvesting using Single inductor Multiple output regulators (SIMO)
    - Peak inductor current control scheme for efficiency
  - SIMO with on-chip caps for PDVS
  - A model for accurate power management study

Outline

- ULP On-Chip Clock Source
- A sub nW 32.768 kHz Crystal Oscillator
- A 50nW Clock Data Recovery Circuit
- Energy and Power Management Solution for ULP SoC
- A Model for Power Management Techniques
- Schedule

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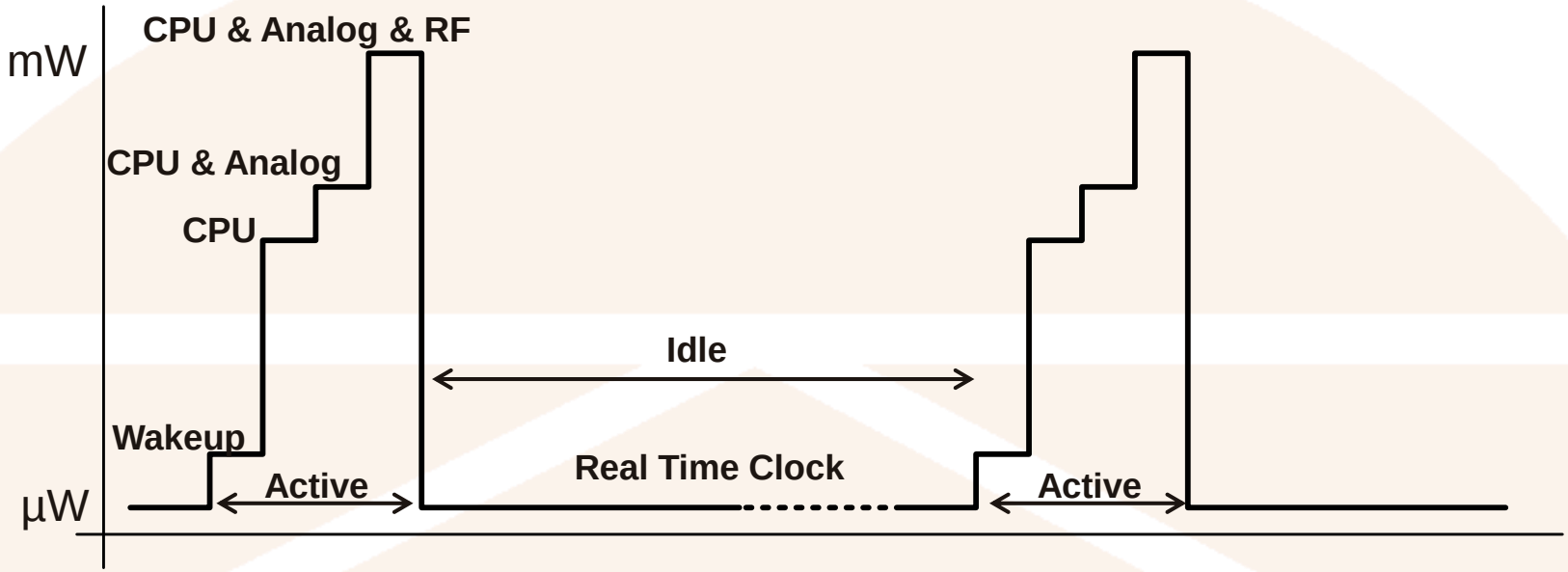
Need for low power Clocking

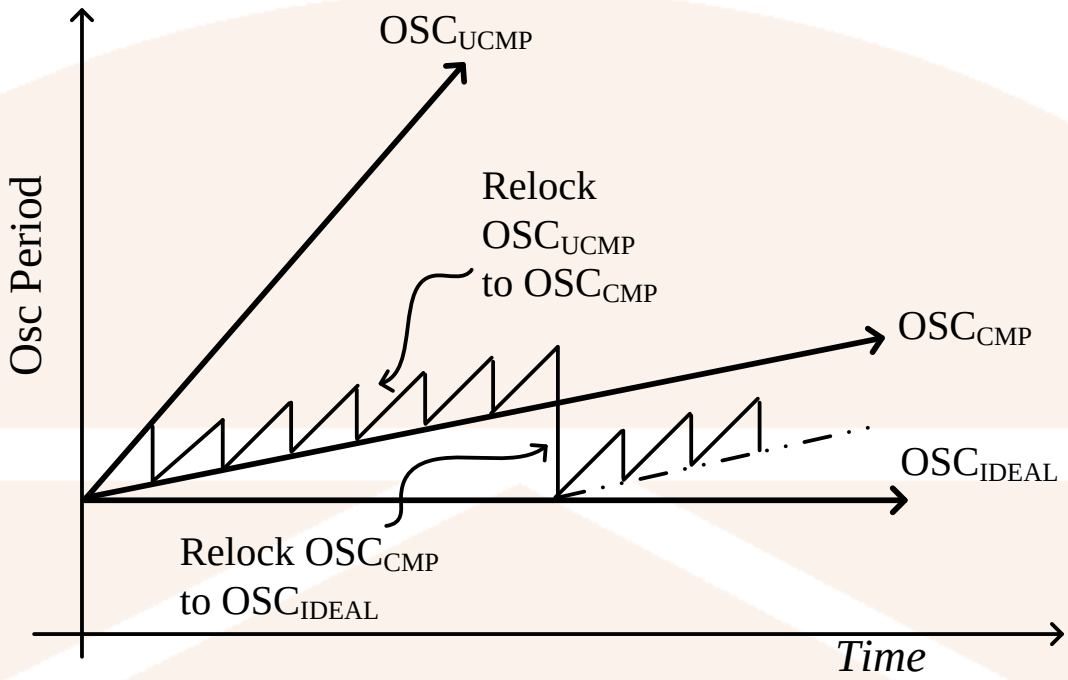


- Power consumption often determined by the clock source
- Uses crystal oscillator for its higher stability.
- Xtals use 3-4 off-chip passives, higher cost, often higher power.
- **In this work we present an on-chip alternative to xtals**

On-Chip Oscillator

- Stable on-chip oscillator has been reported in literature
  - ex :-Y. Tokuyanga, S. Sakiyama, A. Matsumoto, S. Dosho, "An On-chip CMOS Relaxation Oscillator with Voltage Averaging Feedback," *IEEE Journal on Solid State Circuit*, June 2010. stability of 60ppm/^{o}C
- However, to make it stable, temperature compensation is needed → Higher Power
- A lower power uncompensated oscillator can easily be obtained on-chip.
- **This work presents a design where a lower power uncompensated oscillator (OSC_{UCMP}) is used in conjunction with compensated oscillator (OSC_{CMP})to keep the power low with high stability.**

Design Concept

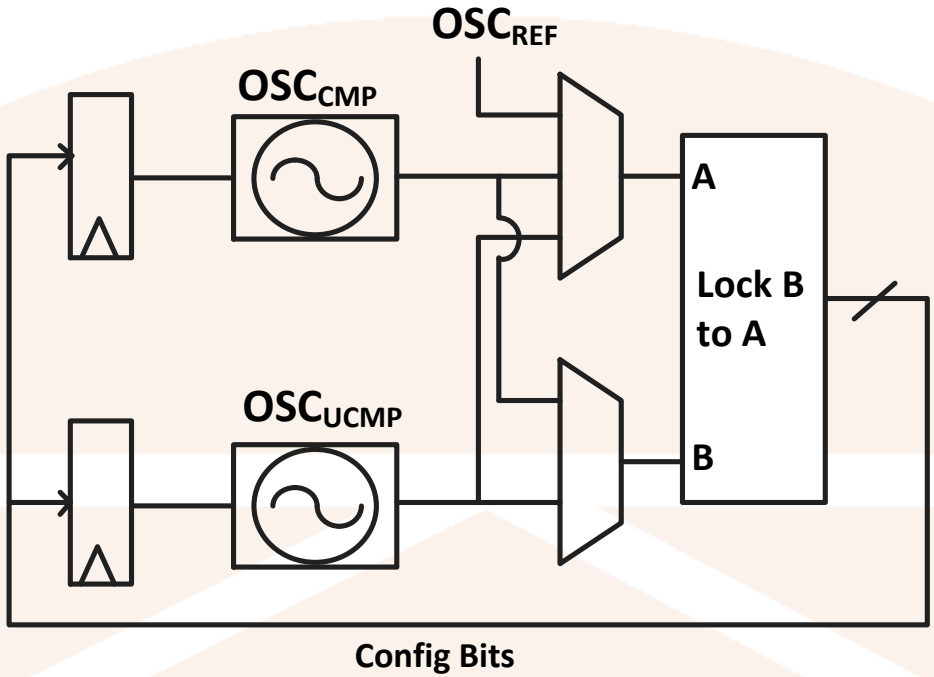


Scheme of re-locking low stability Oscillator to achieve high effective stability

- Locking OSC_{UCMP} often with OSC_{CMP} the error in OSC_{UCMP} can be made very small.
- In between locking time OSC_{CMP} shuts down saving pwr.

- **This way we achieve power of OSC_{UCMP} with the stability OSC_{UCMP} for the clock.**

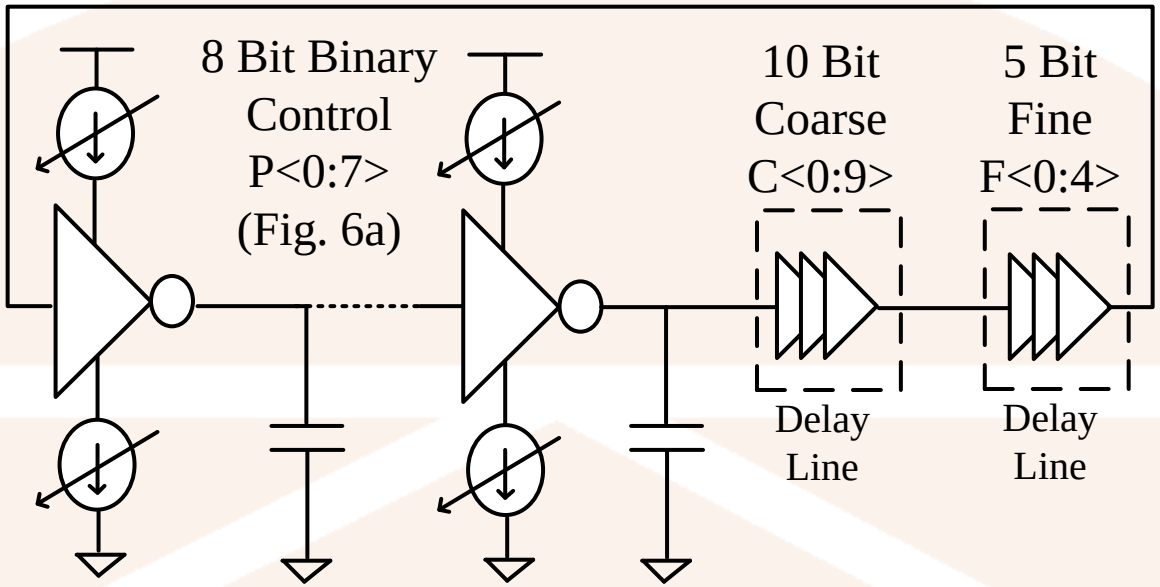
Architecture



- A fast locking circuit to lock OSC_{UCMP} to OSC_{CMP} is also designed.
- If an ideal clock source (ex- xtal, signal over RF) is available OSC_{CMP} can be relocked to that as.

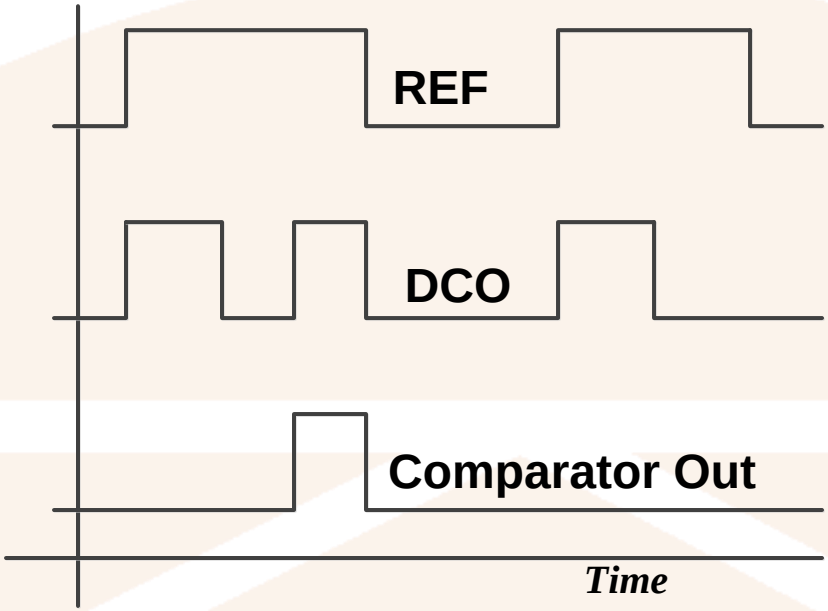
- **We designed OSC_{CMP} , OSC_{UCMP} and a fast locking circuit for the clock system.**

Digitally Controlled OSc



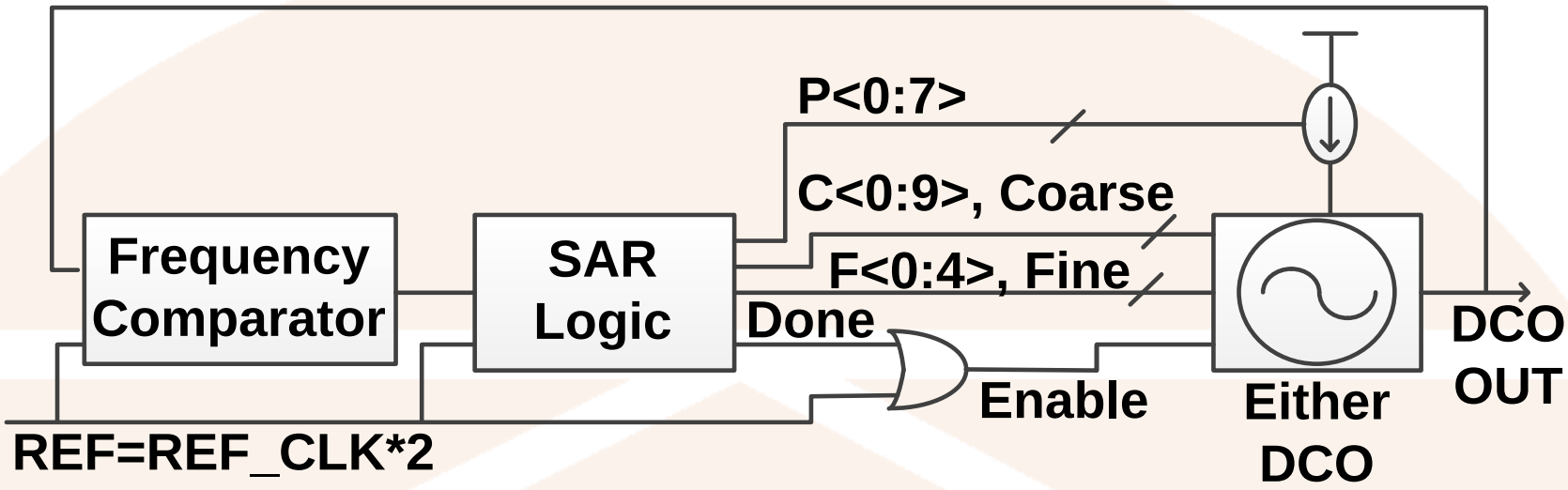
- The binary bit control helps us to get close to reference frequency. We use another 10bit coarse and 5 bit fine delay lines.
- This brings OSC_{CMP} output close 20ps of reference. It is 23 bit DCO. Consumes a µW
- Same structure for OSC_{UCMP}. Consumes 100nW.

Fast Locking Circuit



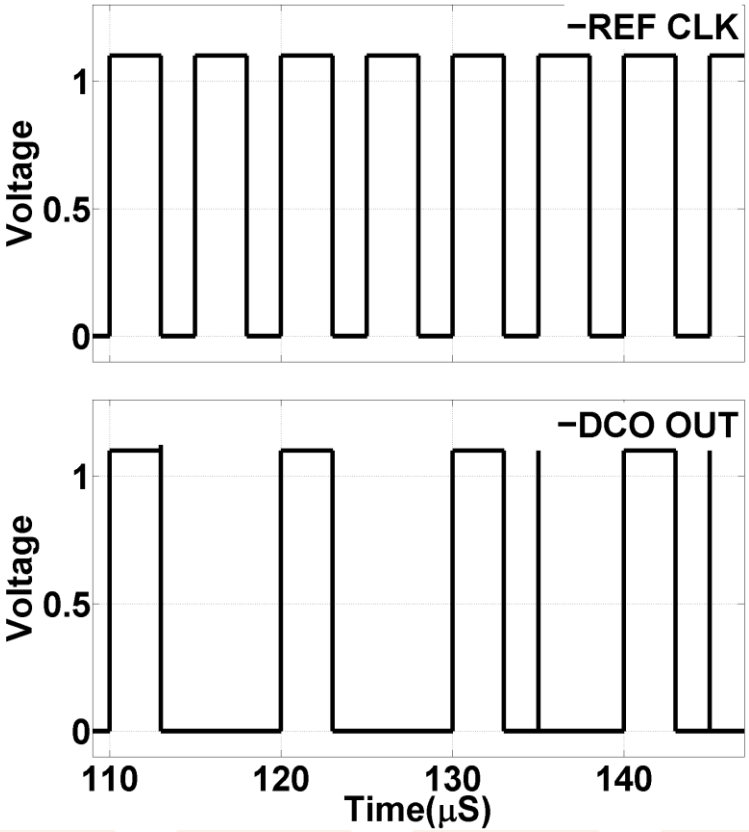
- Heart of locking circuit has a frequency comparator.
- Reference clock is divided by 2 and fed to the frequency comparator. At the rising edge of Ref DCO is enabled.
- Frequency comparator counts number of rise transitions of DCO.
- It signals High if DCO o/p has more than 1 rise transitions.

Fast Locking Circuit

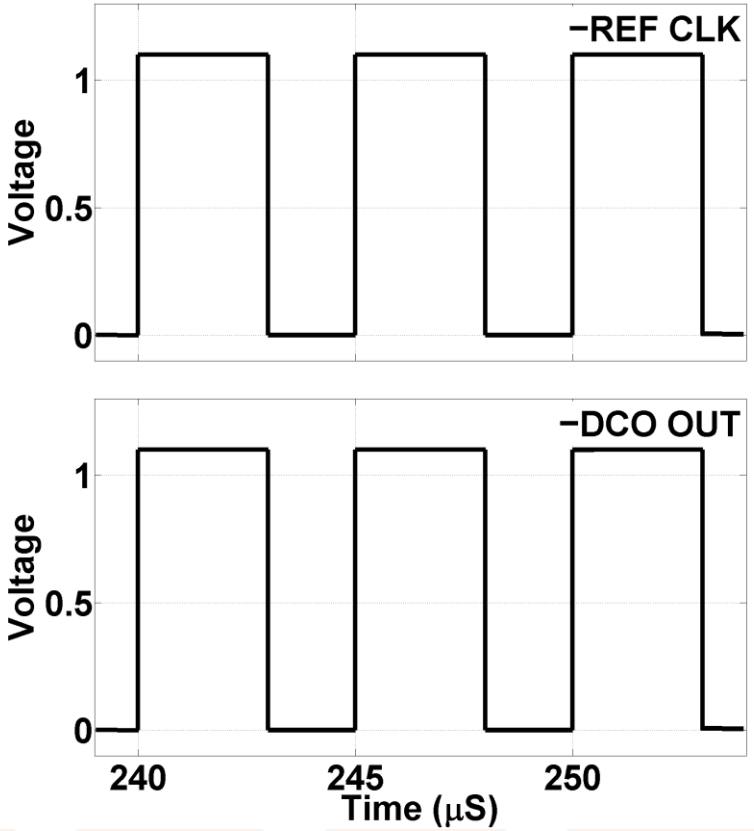


- The comparator output is given to SAR logic which approximates the current and delay inside every alternate cycle.
- It calibrates the DCO o/p to reference within 20pS
- Once the calibration is done, Done goes high DCO starts running on its own. High power reference can be disabled.

Fast Locking Circuit



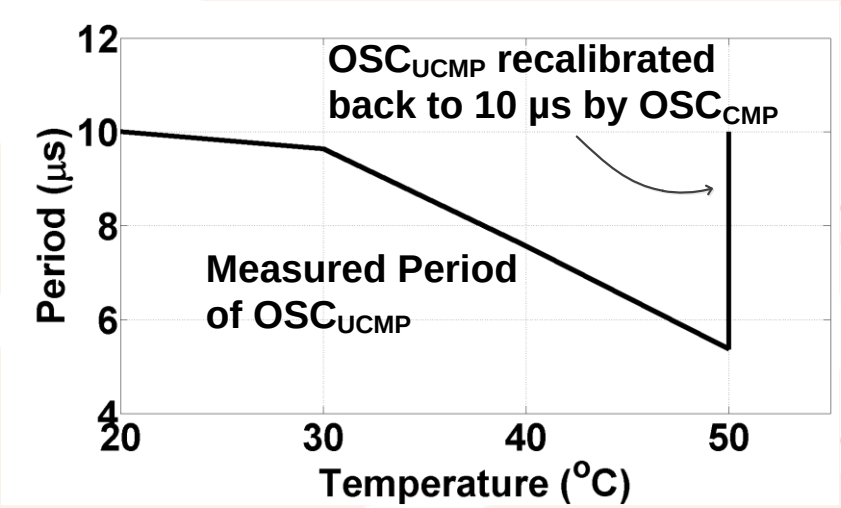
Calibration Transient



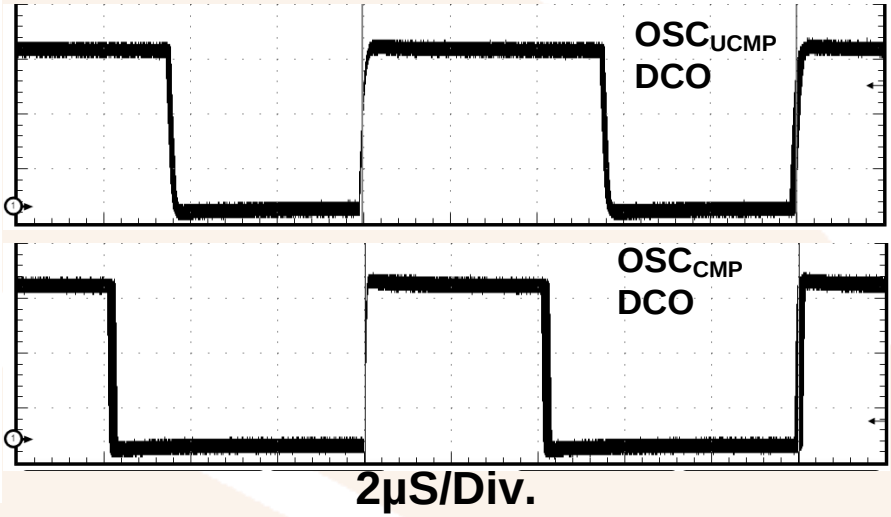
Final Output

- **Simulation result showing calibration transient and final o/p. DCO out is locked within 20ps.**

Measurement Results



a) Recalibration of OSC_{UCMP} with OSC_{CMP}



b) Measured Waveform of DCO outputs at 100khz after re-calibration

Figure shows the recalibration process and waveform of OSC_{UCMP} with OSC_{CMP}

Osc consumes 150nW at 5ppm/°C stability

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- **A sub nW 32.768 kHz Crystal Oscillator**
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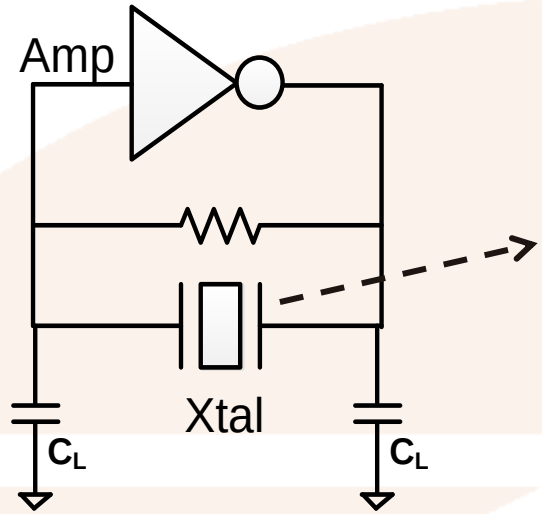
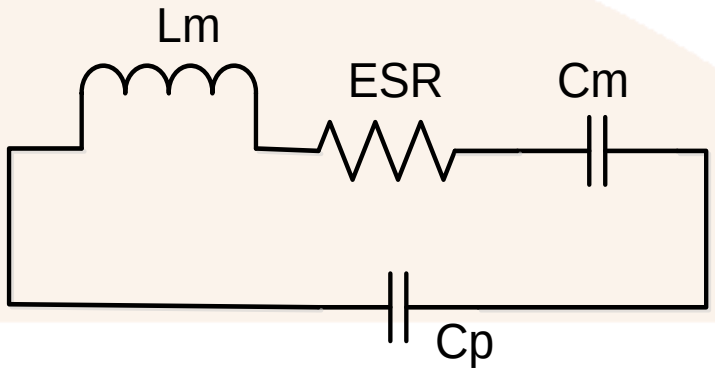
Crystal Oscillator



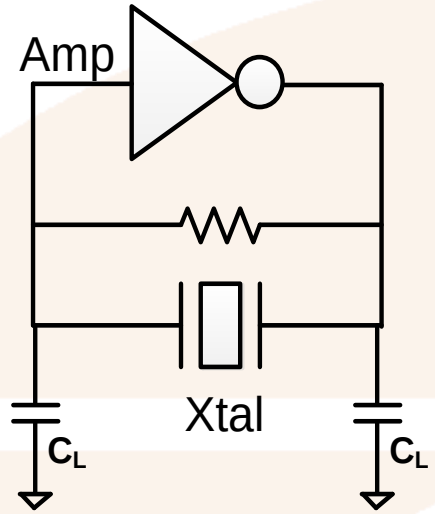
Crystal Oscillator (Xtals)



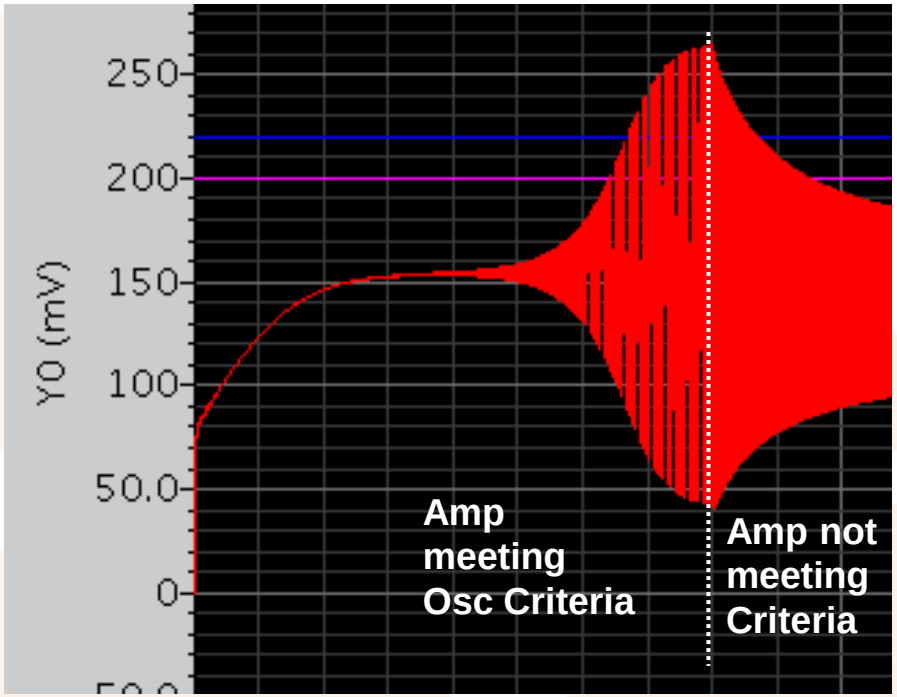
Equivalent Circuit of Xtal

- Xtal is an electromechanical resonator, Provide precise frequency, independent of variations.
- ESR is the damping element responsible for power dissipation. I^2R loss.
- The frequency given by Lm and Cm. 32.768 kHz XTAL is used for Real time clocks.
- **Consumes a µW to 100nW**

Crystal Oscillator

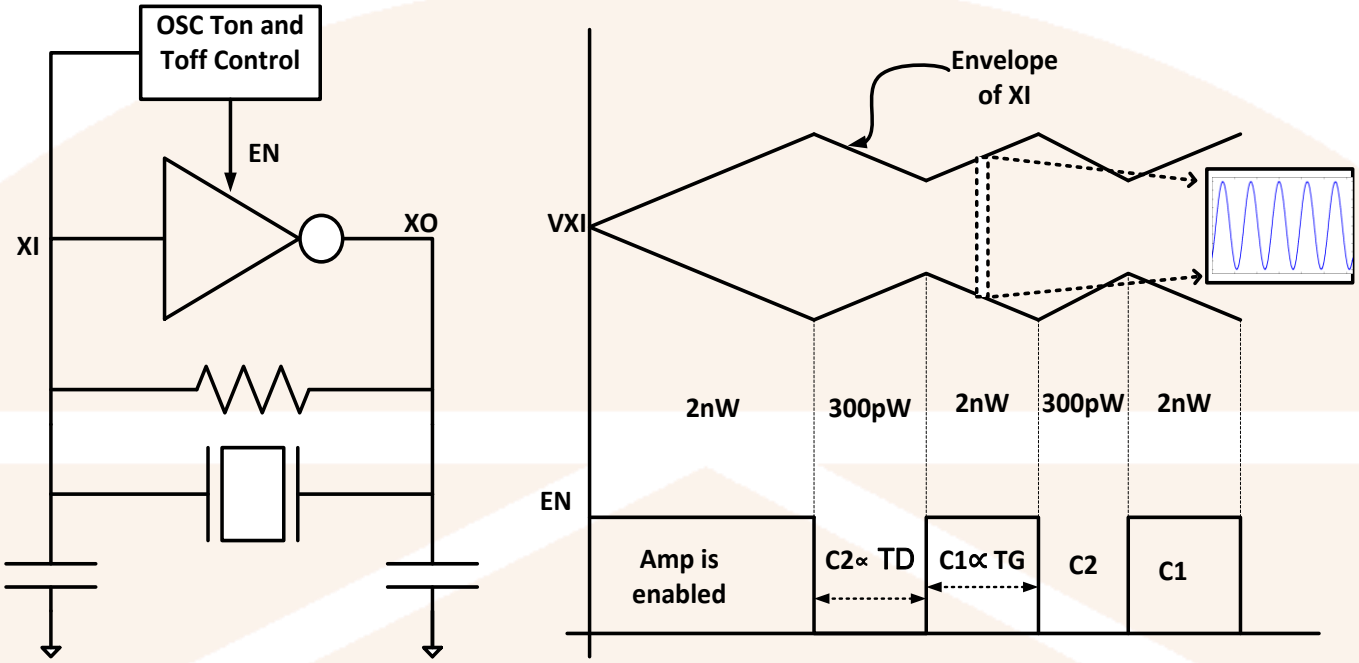


Crystal Oscillator (Xtals)



- Amp provides the negative resistance $R_{Negative}$.
- $R_{Negative}$ > ESR overcomes damping. Causes oscillation
- Higher value of $R_{Negative}$ causes higher power dissipation.
- If amp is disabled, Oscillation decays but can still be detected till amplitude > 50mV, lower power.

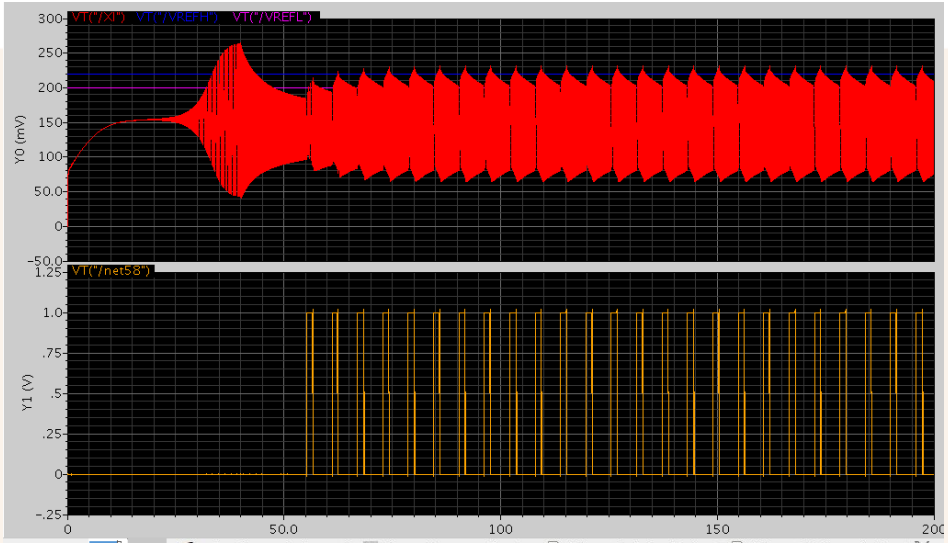
Proposed ULP Crystal



- Xtal is operated at 0.3V VDD to reduce power
- Further power is saved by duty-cycling the amp
- Rise time (TG) and fall time (TD) of Xtal is evaluated
- A Clock with C2∝TD and C1∝ TG is obtained.
- **Power of oscillator brought to <1nW**

Proposed contributions

- A sub-threshold crystal oscillator design.
- A mixed-signal scheme that obtains the TG and TD of a crystal oscillator
- A control scheme where amplifier can be disabled, yet oscillation can be retained utilizing the stored energy in the crystal resonator.
- A ULP level converter circuit for the conversion of crystal output at higher digital voltage



- **Works in simulations**
- **Chip fabricated, awaiting measurement results**
- **Can increase life-time by an order of magnitude**

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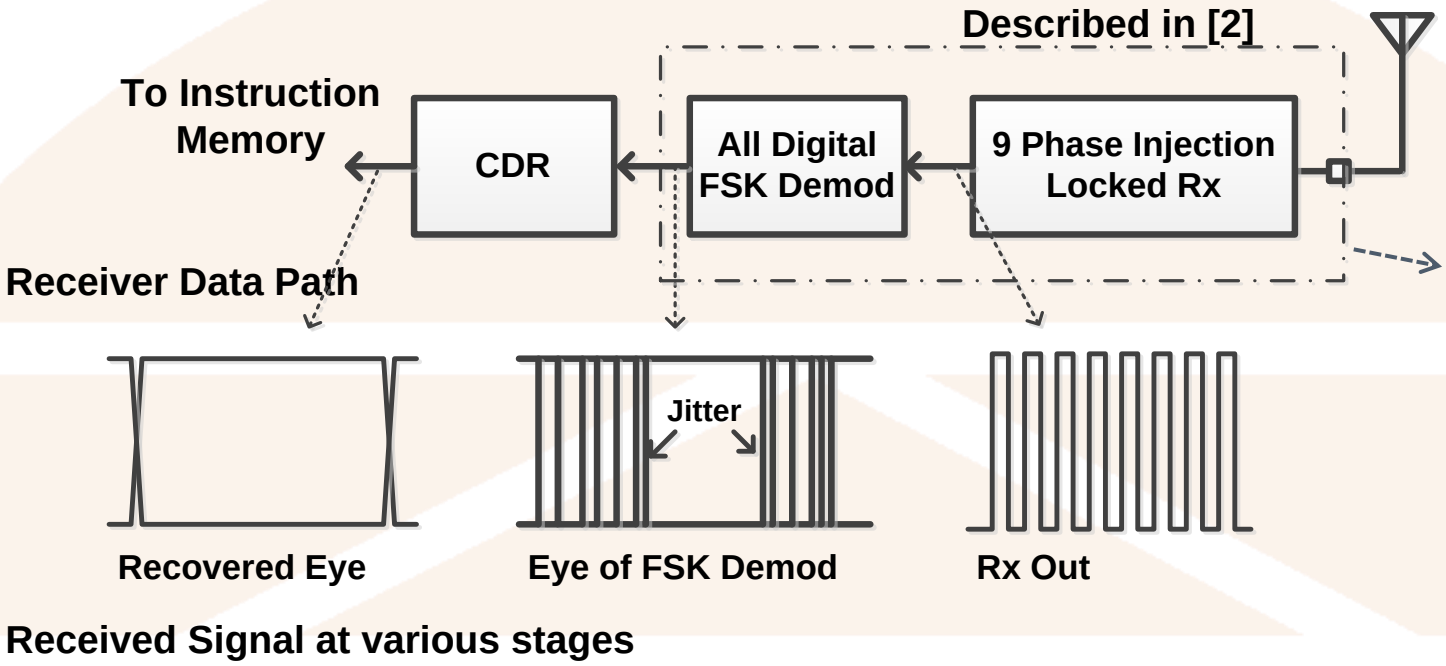
BSN RF Receiver

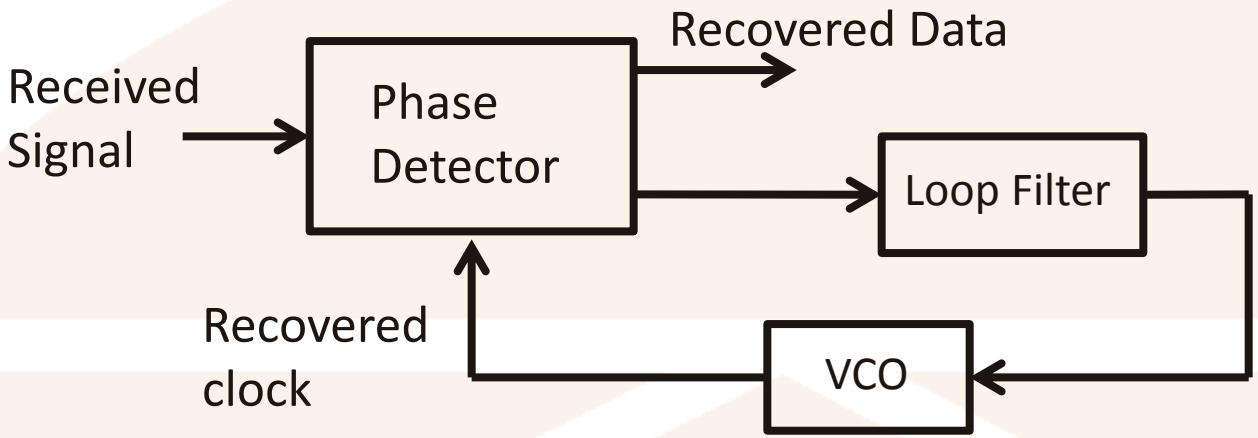


- RF data received in presence of noise.
- Introduces jitter
- **Clock and data recovery needed to recover data for digital processing**

CDR Requirements for BSN

- Conventional approach in designing CDR usually involves a design of PLLs or DLLs
- These solutions are too expensive in terms of area and power for a BSN. Ex:- [11] uses PLL with 110µW Power >> our SoC Power of 19µW.
- All digital FSK Demod is used in [9] to save power
- A low power, lower cost and lower area CDR circuit is needed for BSN

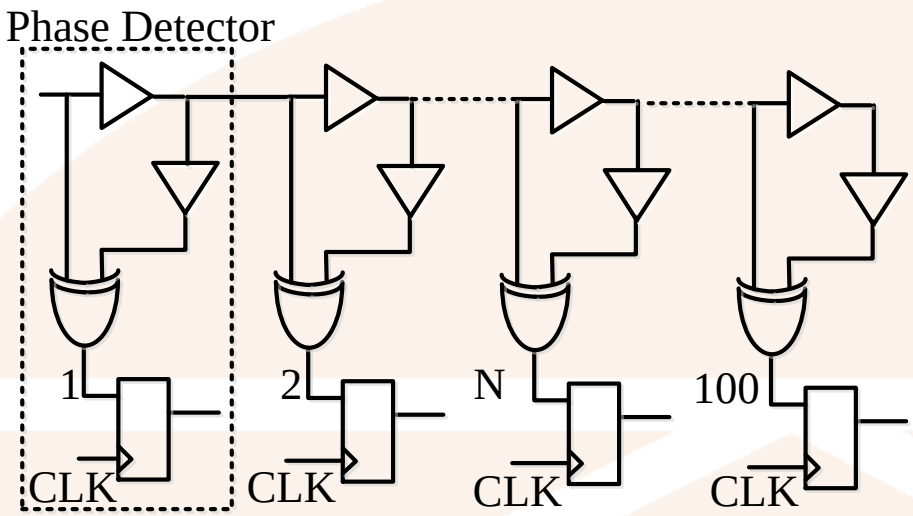
Clock Recovery

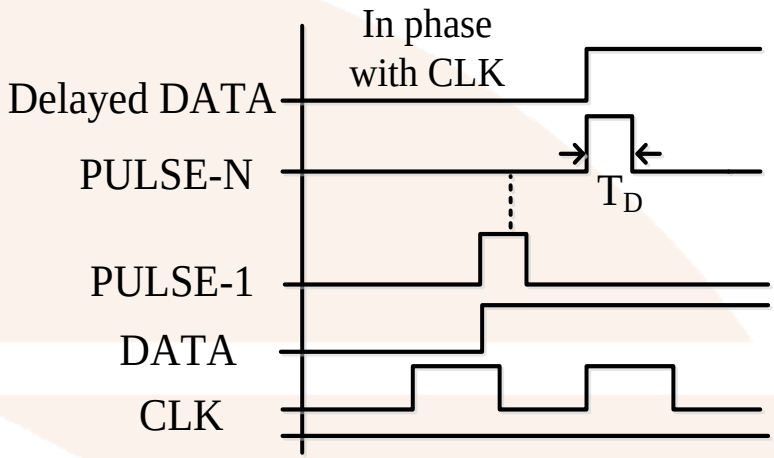


Conventional CDR

- Conventionally CLk is recovered from signal, uses PLL
- In our BSN, Data at 100kB/s, 200khz XTAL for Tx
- Also SoC clock for DSP 200khz from XTAL.
- **SoC clock is used to recover data, eliminating a PLL.**

Data Recovery →Phase Detection





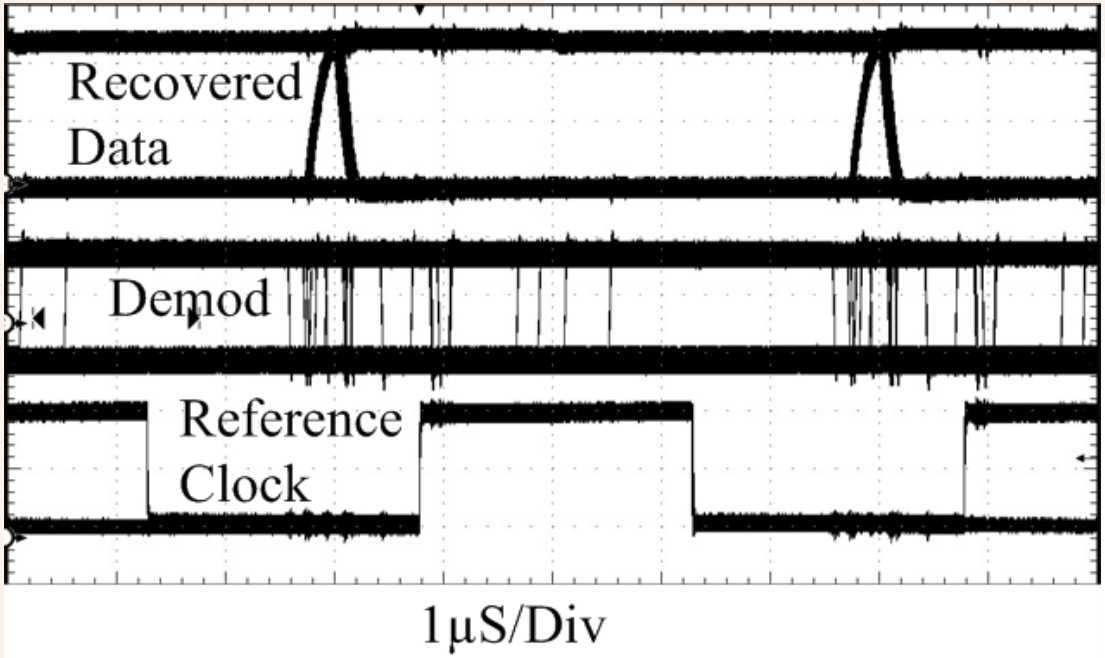
- Pulse generated at each point in delay line.
- Feeds to D-Flip Flop (DFF) clocked at 200 kHz.

- **The pulse close to the edge of the clock will be caught by FF. Point indicating data in phase with clock**

- A number of these phase detectors are placed in series

Contributions

- An easily synthesizable CDR circuit for BSNs.
- Design tradeoff between sensitivity, power, and area.
- Data recovery in the absence of a PLL or DLL
- Circuit consumes 50nW, best reported per bit power consumption



Measured result showing data recovery with more than 2µs jitter from the o/p or receiver

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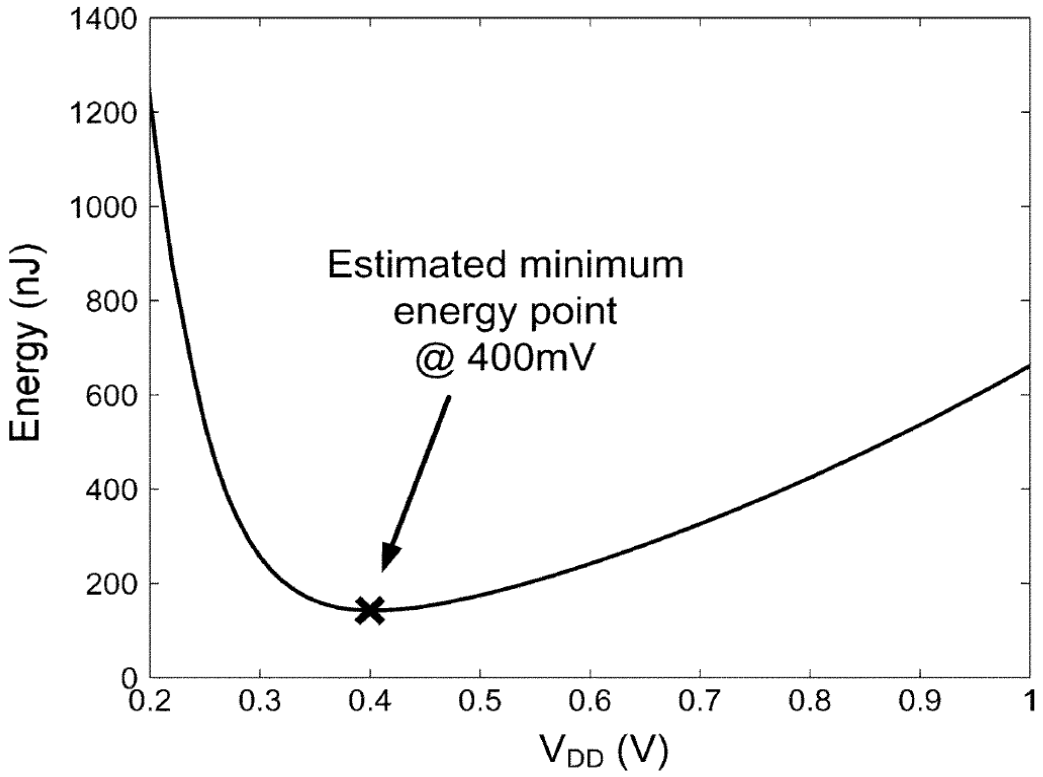
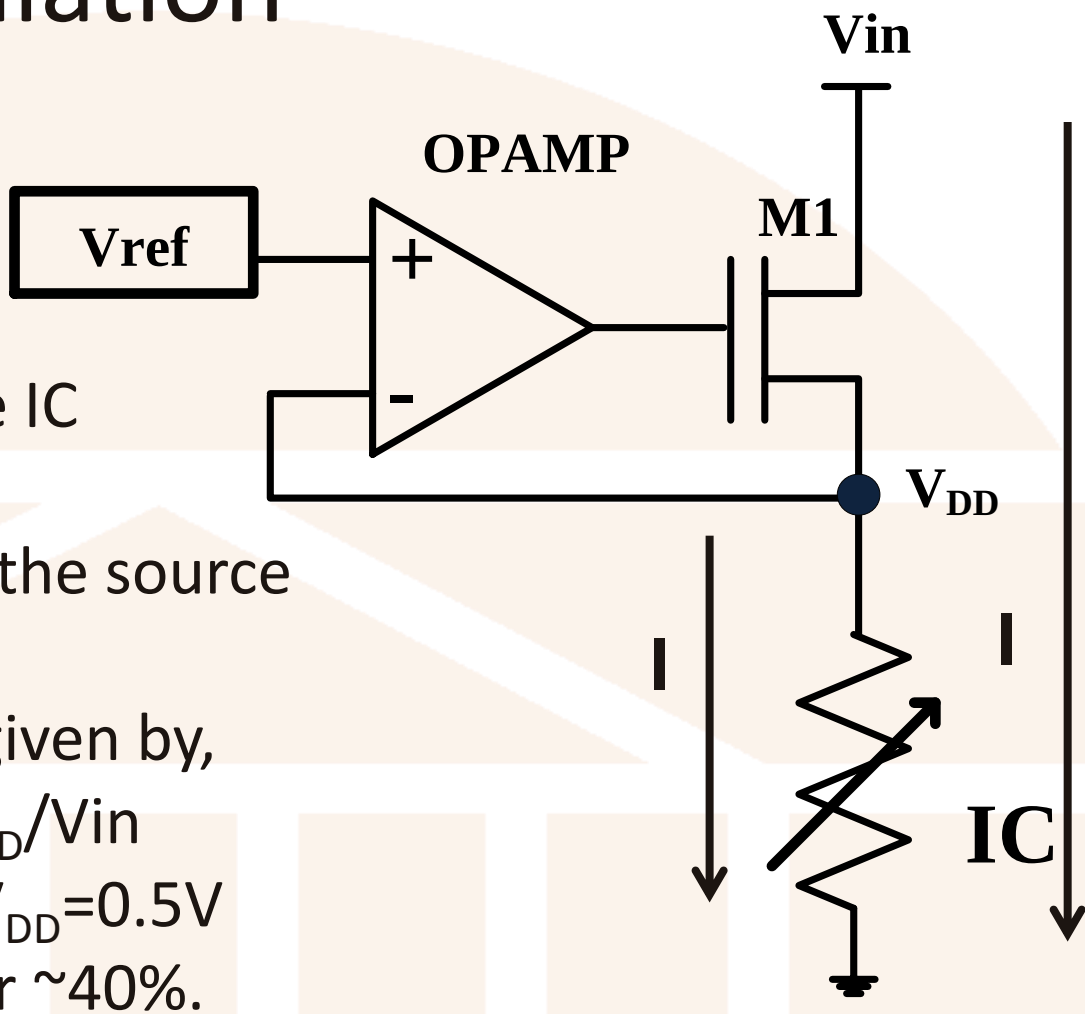
Power Supply Needs



A. Wang, et al, "A 180-mV Subthreshold …" *JSSC*, Jan. 2005

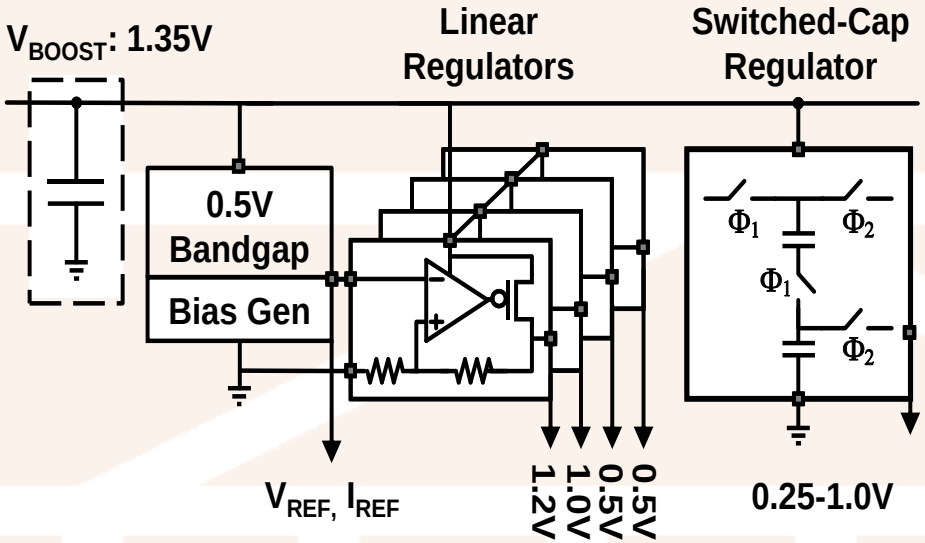
- Optimal energy point exists for each blocks such as CPU, Analog, RF etc.
- Multiple regulated output voltages is needed.

Voltage Regulation



- Input power to the IC
  - V_{DD}*I
- Power taken from the source
  - Vin*I
- Ideal Efficiency is given by,
  - V_{DD}*I/Vin*I=V_{DD}/Vin
- Ex, Vin=1.2V and V_{DD}=0.5V
- Efficiency is 0.41 or ~40%.
- **Almost 60% of power is lost in regulation**

State of the art BSN SoC Power Management

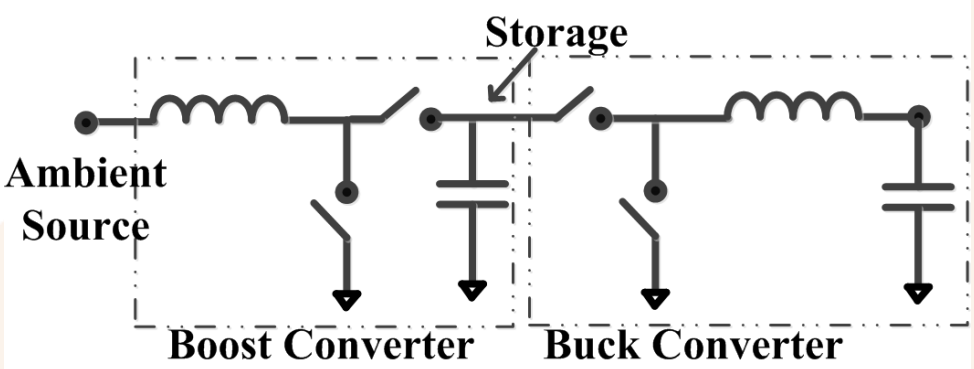


Voltage Domain	Blocks Powered
1.2V	Pads, AFE
1.0V	TX LO
0.5V	TX PA
0.5V	DPM, MEM, Accels
SC Reg. (0.25-1.0V)	Accels for DVS

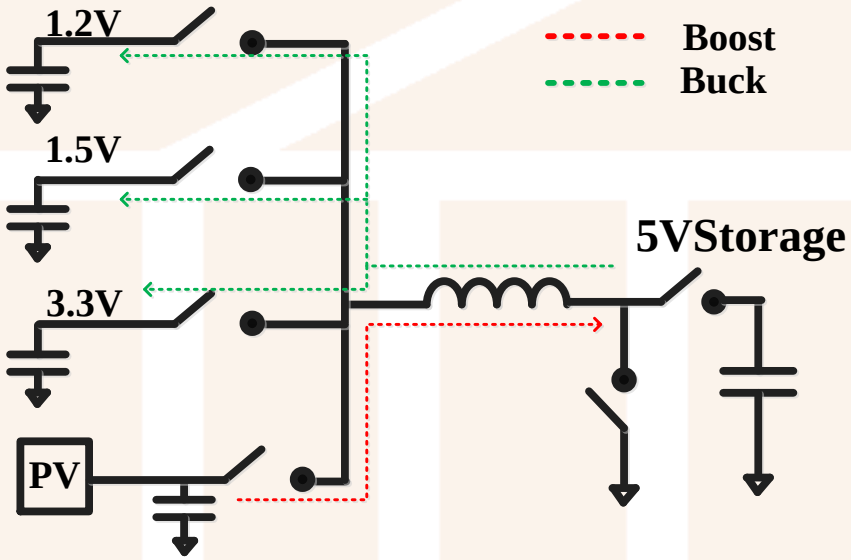
Y. Zhang, et al, "A Batteryless 19uW…. ", JSSC, Jan. 2013.

- Boost converter harvests the energy on to a capacitor at 1.35V
- Multiple rails are served by linear regulators
- **63% 23% and 12% energy is lost in voltage regulation.**

Recent solution for BSN



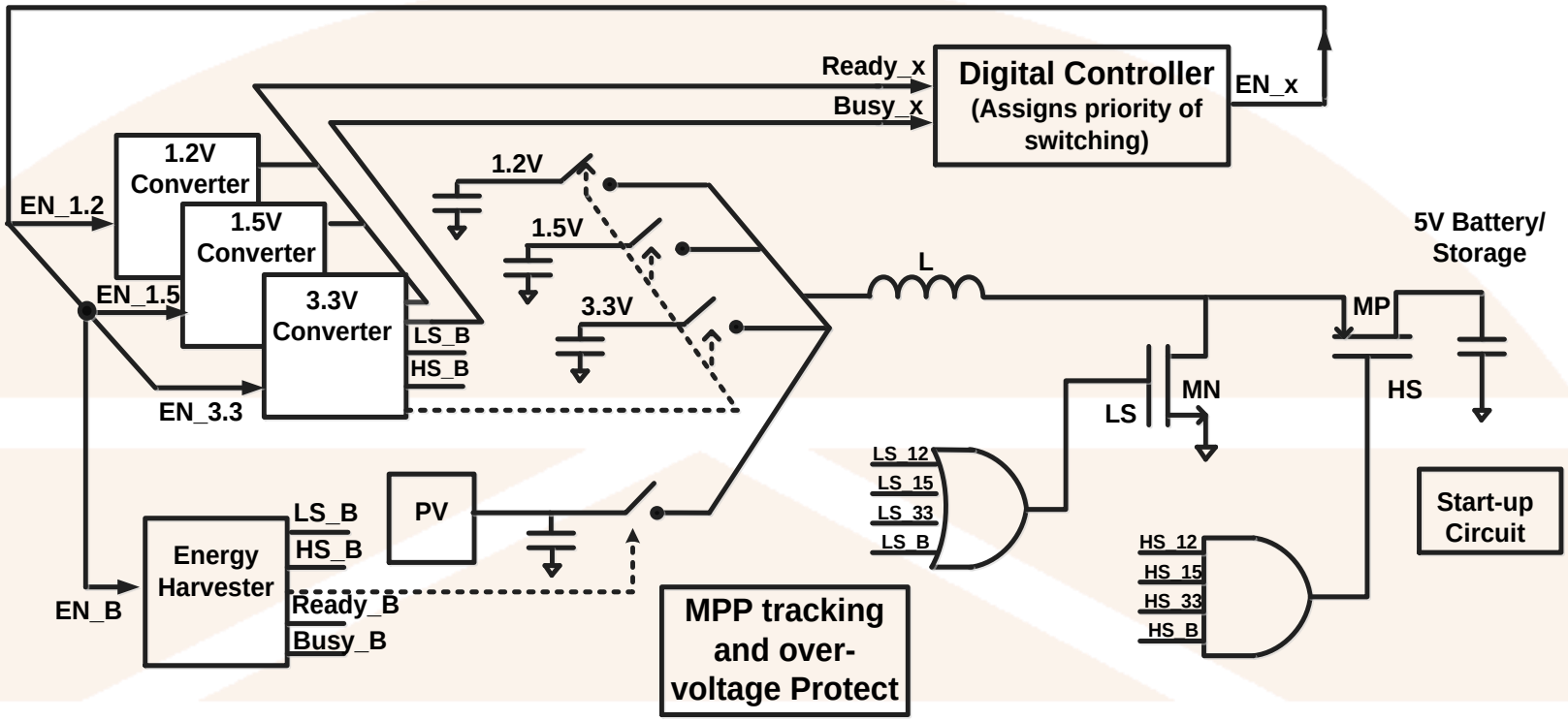
State of the art Energy Harvesting Solution
K. Kadrivel et al, "A 330nA Energy ...." ISSCC2012



Proposed Energy Harvesting Solution

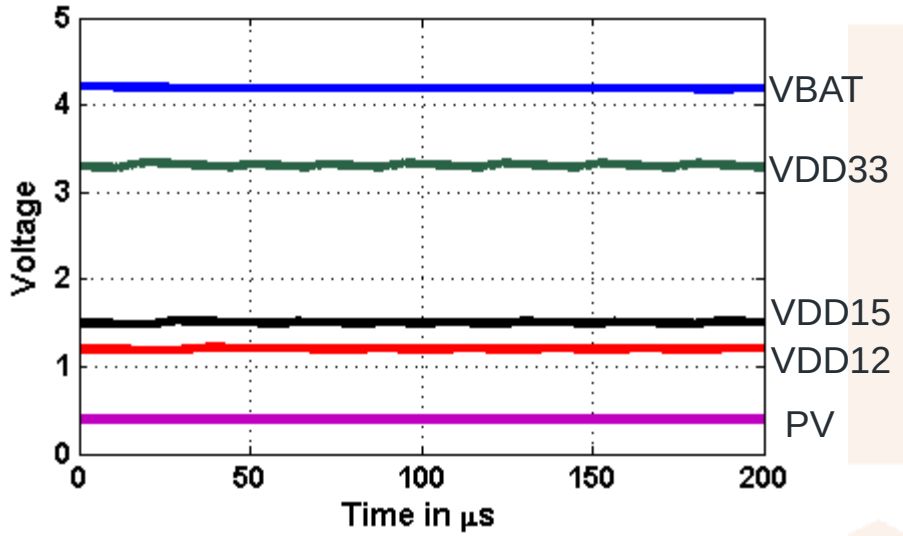
- DC DC converter can be used for higher efficiency
- BSN SoC needs multiple VDDS, which comes from LDOs (efficiency↓)
- Multiple DC-DC converter will increase cost.
- Single inductor energy harvesting and power management circuit.

Proposed Architecture

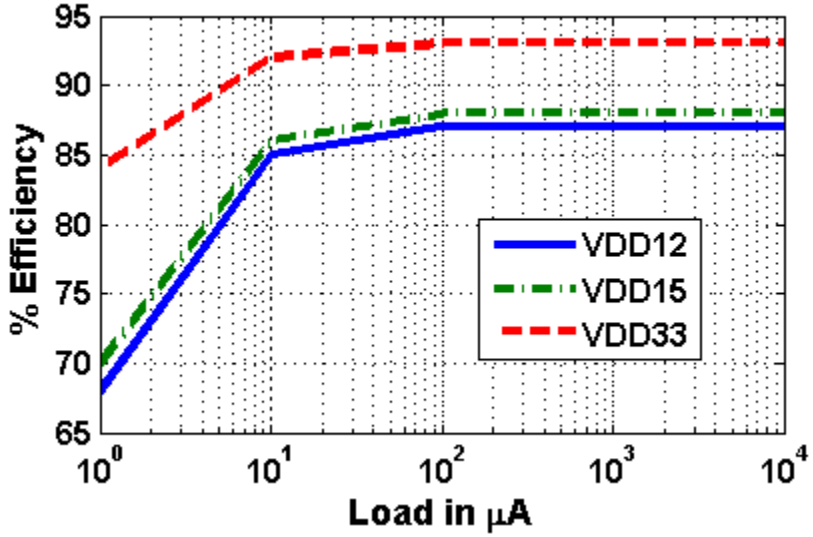


- Multiple DC-DC converter are implemented using a single inductor.
- Each converter is time division multiplexed.
- Digital controller controls a converter by using Busy and Ready signals and priority, based on the load profile.

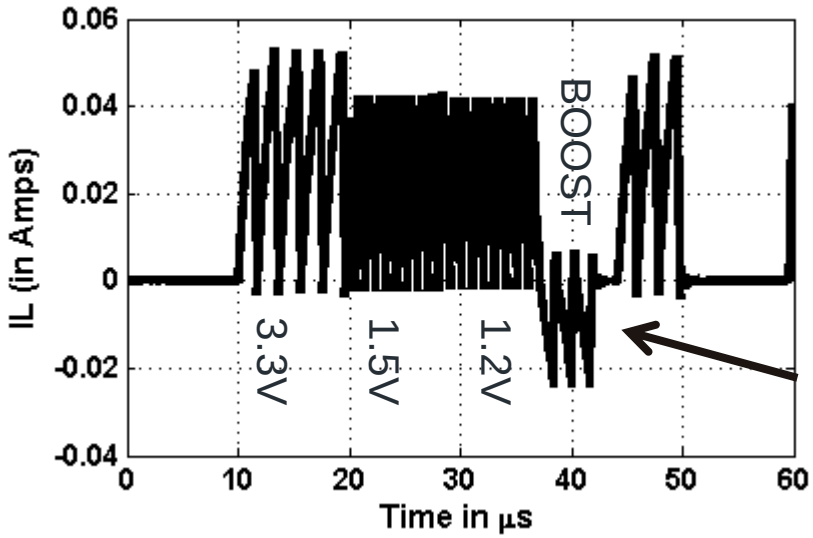
Simulation Results



Rails at 5mA load with 0.4V 100µA PV

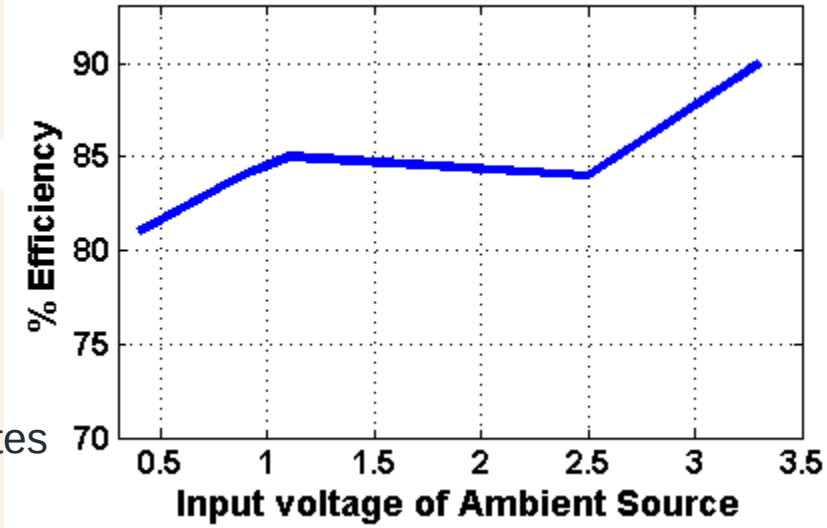


Efficiency of Buck Converters



-ve IL indicates boost

Inductor current serving all the rails



Efficiency of Boost Converter

Proposed Contributions

- Single inductor energy harvesting and power management interface.
- A peak inductor current control scheme to increase the efficiency.
- A high voltage battery support for the energy harvester.
- A high efficiency energy harvester for TEG to utilize body heat.
- An offset compensating zero detection scheme.
- A SIMO with on-chip capacitors for PDVS.
- A hysteretic comparator control scheme for DC-DC converter with on-chip decoupling capacitor.

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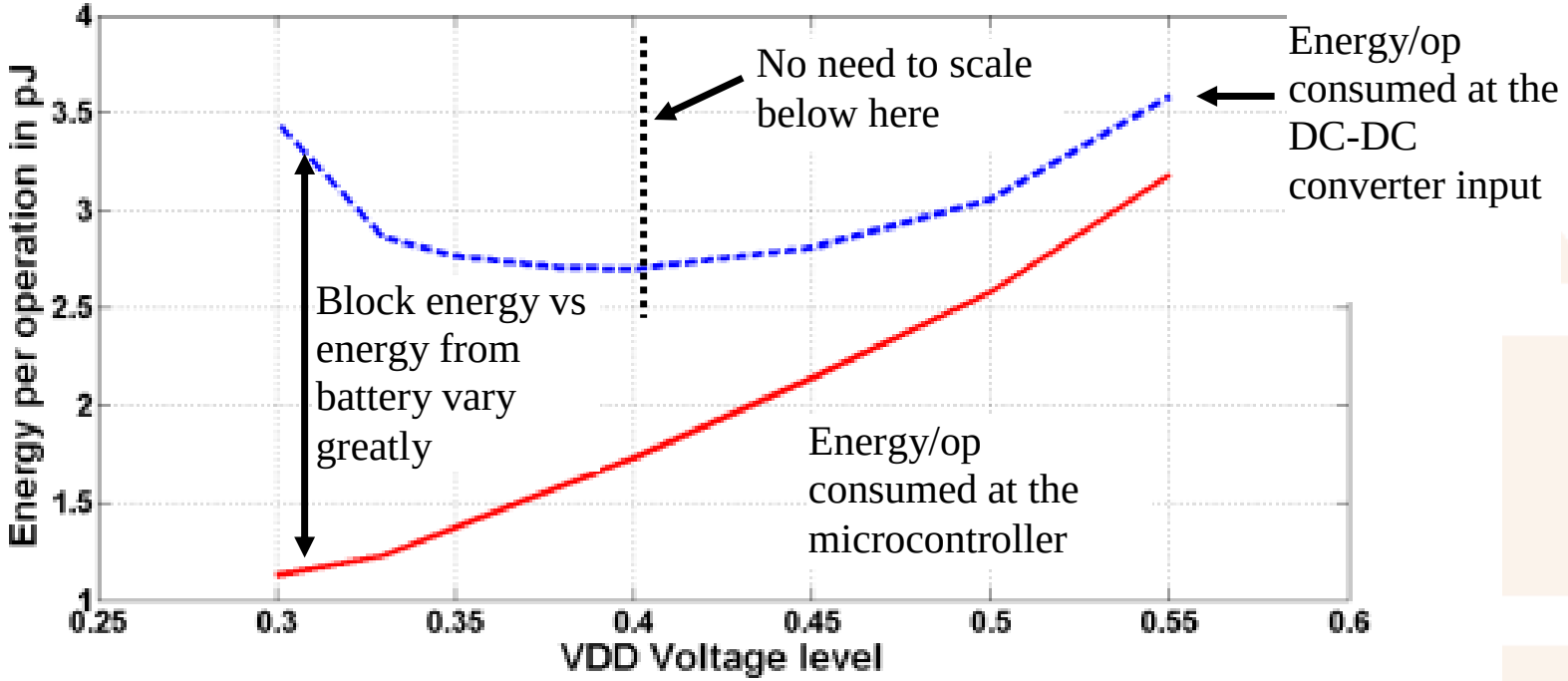
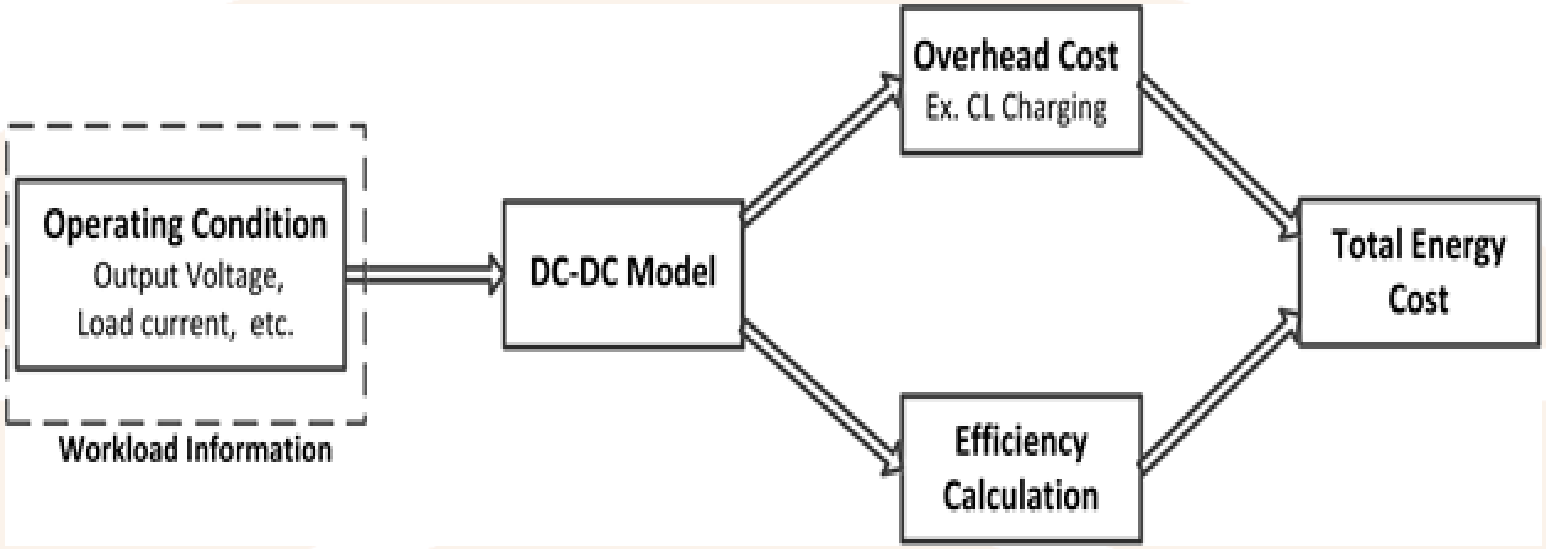
Need to study power management with DC-DC



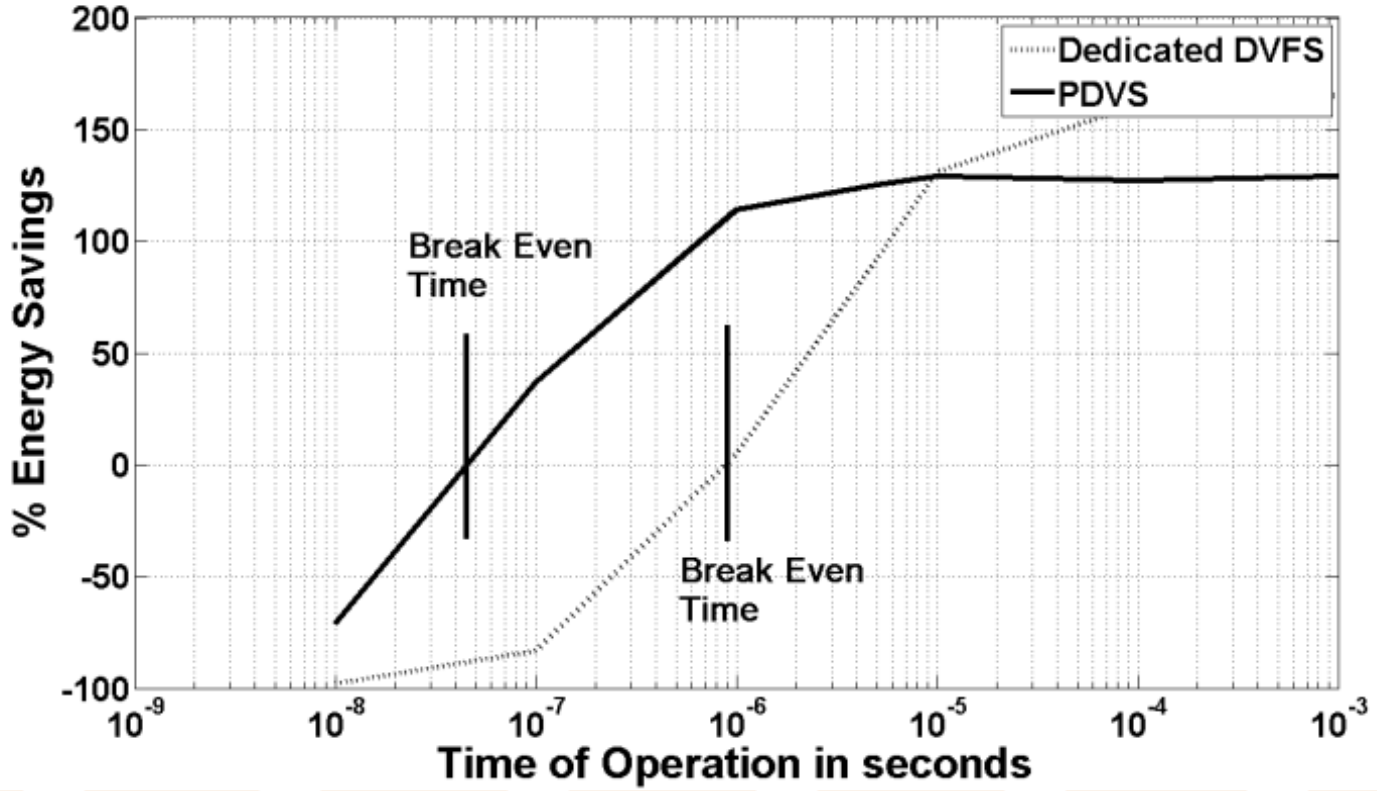
- DC-DC impacts the savings reported from DVFS etc.
- Overheads such as change in eff. with changing loads etc can offset the benefits.
- Model provides the framework to calculate the benefits accurately

Proposed contributions



- Model of DC-DC converter across varying topology.
- Framework to obtain energy cost.
- Evaluation of various power management techniques in a dynamic work load environment.

Evaluation of Power Management techniques



- No benefits if Power management is done often
- PDVS better to implement higher rate of DVS

Schedule

Subject	#	Task Description	Status/Target	Publications
ULP-On Chip Clock Source	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	
	4	Test Chip	Done	[AS_P4]
	5	Silicon Validation	Done	[AS5] [AS2][AS7][AS16]
ULP 32.768 kHz Crystal	1	Design Exploration	Done	[AS_P5]
	2	Simulations	Done	
	3	Schematic/Layout	Done	
	4	Test Chip	Done	
	5	Silicon Validation	June 2013	[AS14][AS15][AS16]
CDR	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	[AS8]
	4	Test Chip	Done	
	5	Silicon Validation	Done	[AS1] [AS2][AS7]
DC- DC Model	1	Design Exploration	Done	
	2	Model generation	Done	
	3	Coding	Done	
	4	Model Validation	Done	[AS4][AS10]
Energy Harvesting and Power Management Interface	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	[AS3] [AS_P1] [AS_P2]
	4	Test Chip #1	Done	[AS_P3]
	5	Test Chip #2	Done	
	6	Test Chip #3	Done	
	7	Silicon Validation #1	Done	[AS9]
	8	Silicon Validation #2	June 2013	[AS11][AS12]
	9	Silicon Validation #3	August 2013	[AS13]
Write up	1	Thesis Writing	Nov 2013	

Current Publications

- [AS1] **A. Shrivastava**, and B. H. Calhoun, “A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node” VLSI Design Conference. Jan. 2013.
- [AS2] Y. Zhang, F. Zhang, Y. Shakhsheer, J. Silver, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, **A. Shrivastava**, et al., "A Batteryless 19 uW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications “, Journal of Solid State Circuit, Jan. 2013.
- [AS3**] A. Shrivastava**, Y. Ramadass, S. Bartling and B. H. Calhoun, “Single Inductor Energy Harvesting and Power Management Circuit for Body Sensor Nodes”, ISSCC SRP 2013.
- [AS4] **A. Shrivastava**, and B. H. Calhoun, “Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems"” Sub-threshold Conference Oct-2012.
- [AS5] **A. Shrivastava**, and B. H. Calhoun, “A 150nW, 5ppm/o C, 100kHz On-Chip Clock Source for Ultra Low Power SoCs” Custom Integrated Circuits Conference. Sept. 2012.
- [AS6] **A. Shrivastava**, J. Lach, and B. H. Calhoun, “A Charge Pump Based Receiver Circuit for a Voltage Scaled Interconnect” International Symposium on Low Power Electronics and Design, Jul. 2012
- [AS7] F. Zhang, Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, **A. Shrivastava**, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", International Solid State Circuits Conference, Feb. 2012.
- [AS8] **A. Shrivastava**, and B. H. Calhoun, “A sub-threshold clock and data recovery circuit for a wireless sensor node”, Sub-threshold Conference. Sept. 2011.

Anticipated Papers

[AS9] SIMO for PDVS paper submitted to VLSI
[AS10] DC-DC Model, journal article submitted to JLPEA
[AS11] Energy Management and Harvesting, [conference paper]
[AS12] Energy Management and Harvesting, [Journal]
[AS13] TEG based boost converter
[AS14] ULP XTAL oscillator
[AS15] BSN chip rev-2
[AS16] Clock chip system

Patents

[AS_P1] **A. Shrivastava**, and Y. Ramadass, "Apparatus and Method for Controlling Peak Inductor Current in a Switched Mode Power Supply" US Patent application 13768448
[AS_P2] **A. Shrivastava**, Y. Ramadass, and S. Bartling, "Single Inductor Energy Harvesting and Management Interface System and Method" US Patent application
[AS_P3] **A. Shrivastava**, and B. H Calhoun, "Single Inductor Multiple Output (SIMO) Step-down DC-DC Converter for Ultra Low Power SOCs" US Patent application 61/700979
[AS_P4] **A. Shrivastava**, and B. H. Calhoun. US Patent Application 61/698,534. "On-Chip Clock Source for Ultra Low Power SoCs"
[AS_P5] **A. Shrivastava**, et al, US Patent 8120439 "A Fast Start-up Crystal Oscillator"

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- [2] A. Wang, and A. Chandrakasan, “A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology” IEEE Journal on Solid State Circuit, Jan. 2005
- [3] Y.-S. Lin, D. Sylvester, and D. Blaauw, “A Sub-pW Timer Using Gate Leakage for Ultra Low-Power Sub-Hz Monitoring Systems,” IEEE Custom Integrated Circuits Conference, Sept. 2007
- [4] Y.-S. Lin, D. Sylvester, and D. Blaauw, “A 150pW program-and-hold timer for ultra-low-power sensor platforms” IEEE International Solid State Circuits Conference, Feb. 2009
- [5] Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, “A 660pW Multi-stage Temperature Compensated Timer for Ultra-low Power Wireless Sensor Node Synchronization”, IEEE International Solid State Circuits Conference, Feb. 2011
- [6] Y. Tokuyanga, S. Sakiyama, A. Matsumoto, and S. Dosho, “An On-chip CMOS Relaxation Oscillator with Voltage Averaging Feedback,” IEEE Journal on Solid State Circuit, June 2010
- [7] W. Thommen, "An Improved Low Power Crystal Oscillator," IEEE European Solid-State Circuits Conference, Sept. 1999
- [8] D. Yoon, D. Sylvester and D. Blaauw, “A 5.58nW 32.768kHz DLL-Assisted XO for Real-Time Clocks in Wireless Sensing Applications”, IEEE International Solid State Circuits Conference, Feb. 2012
- [9] J. Pandey, S. Jianlei and B. Otis, “A 120µW MICS/ISM-band FSK receiver with a 44µW low-power mode based on injection-locking and 9x frequency multiplication”, IEEE International Solid State Circuits Conference, Feb. 2011
- [10] T. Kleeburg, J. Loo, N. J. Guilar, E. Fong and R. Amritharajah , “Ultra-low-voltage circuits for sensor applications powered by free-space optics”, IEEE International Solid State Circuits Conference, Feb. 2010
- [11] S-J Song, N. Cho, and H-J Yoo, “A 0.2-mW 2-Mb/s Digital Transceiver Based on Wideband Signaling for Human Body Communications”, IEEE Journal on Solid State Circuit, Sept. 2007
- [12] S. Kim, et. al, “A low-power referenceless clock and data recovery circuit with clock-edge modulation for biomedical sensor applications”, IEEE International Symposium on Low Power Electronics and Design, Aug. 2007
- [13] S. M. Martin, K. Flautner, T. Mudge and D. Blaauw,“ Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads,” International Conference on Computer Aided Design 2002.
- [14] K. Kadrivel, et al, “A 330nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting” IEEE International Solid State Circuits Conference, Feb. 2012
- [15] L. C. Fai, and P. K. T. Mok, “A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique” IEEE Journal on Solid State Circuits, Jan. 2004

Thank You

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